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Docket No.: GR 98 P 8041

MAIL STOP: APPEAL BRIEF-PATENTS

By: Mathias Wille Date: Jan 20, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/313,424 Confirmation No.: 3890
Inventor	:	Thomas Huttner et al.
Filed	:	May 17, 1999
Title	:	SOI Semiconductor Configuration And Method Of Fabricating The Same
TC/A.U.	:	2823.0
Examiner	:	Brook Kebede
Docket No.	:	GR 98 P 8041
Customer No.	:	24131

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

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Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

01/27/2004 MAHMED1 00000007 09313424

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Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention lies in the field of semiconductor manufacture. Specifically, the invention relates to a SOI semiconductor configuration, i.e., a structure formed with a base layer (e.g. substrate) of semiconductor material, an insulation layer on the base layer, and a layer of monocrystalline silicon disposed on and adjoining the insulation layer. The invention also pertains to a method of manufacturing the SOI structure.

Appellants explained on page 12 of the specification, line 14, that, referring now to the figures of the drawing in detail and first, particularly, to Figs. 1a to 1f thereof, there is seen an SOI semiconductor structure 5 that comprises an Si base layer 1, which is formed by an Si substrate and is adjoined by a buried oxide layer 2, on which a monocrystalline silicon layer 3 is overlaid. By way of example, the SOI semiconductor structure 5 may be fabricated according to the SIMOX or BESOI technologies and is commercially available as a finished product. Furthermore, the Si base layer 1 and the monocrystalline silicon layer 3 may already be p- or n- predoped by the manufacturer.

Appellants outlined on page 13 of the specification, line 1, that, with reference to Fig. 1a, a screen oxide layer 4 is first formed on the SOI semiconductor structure 5. The screen oxide layer 4 may be formed for example by thermal oxidation of the monocrystalline silicon layer 3 or by deposition of a TEOS (tetraethylorthosilicate) layer by means of a CVD process.

Appellants further outlined on page 13 of the specification, line 7, that, with reference to Fig. 1b, the passivating substance X is subsequently incorporated in a whole-area or large-area application by implantation into the buried oxide layer 2. The implantation step is illustrated by arrows 6. By way of example, nitrogen, fluorine or chlorine is used as the passivating substance X. The incorporation process can be controlled in a highly targeted manner with regard to the incorporation depth, the incorporation dose and the incorporation profile. Since the passivating substance X is intended to be employed in the region of the interface 7 between the monocrystalline silicon layer 3 and the buried oxide layer 2, conditions which cause the implantation maximum 8 to lie a short way underneath the interface 7 are chosen in the implantation step.

It is stated in the last paragraph on page 13 of the specification, line 22, that a heat-treatment step is subsequently carried out. In the process, the passivating substance X implanted into the buried oxide layer 2 diffuses to the interface 7, the passivating substance distribution 8' also being shifted into the region of the interface 7. In the process, Si-H bonds present in the region of the interface 7 are replaced by the more energy-stable Si-X bonds. As a result, the damage resistance of the buried oxide layer 2 with respect to HC degradation is increased in the manner already described. Furthermore, the heat-treatment step effects annealing of damage or defects which have occurred during the implantation step in the upper layers 3 and 4. Fig. 1c illustrates the situation after the heat-treatment step has been carried out. The concentration of the passivating substance X may be approximately 10^{18} cm^{-3}, for example.

Appellants described on page 14 of the specification, line 12, that Figs 1d to 1f show, by way of example, further process steps which are carried out for the patterning and insulation of the monocrystalline silicon layer 3 for the purpose of forming an SOI MOSFET. Such steps are also necessary to construct an integrated CMOS circuit on the SOI semiconductor structure 5. First of all, in accordance with Fig. 1d, the screen oxide layer 4 and the monocrystalline silicon layer 3

are removed, except for locally residual layer regions 3', 4', using customary photolithographic masking techniques and etching steps. As a result, the monocrystalline layer region 3' is electrically insulated from corresponding, adjacent layer regions (not illustrated in Fig. 1d). The method shown here is known as Mesa insulation in the art. Other insulation methods (for example LOCOS, STI) can also be employed instead of Mesa insulation.

Appellants explained on page 15 of the specification, line 2, that, according to Fig. 1e, the peripheral walls of the layer regions 3', 4' are covered with spacers 9. The spacers 9 serve to additionally insulate the peripheral walls of the free-standing layer regions 3', 4'.

Appellants further explained on page 15 of the specification, line 7, that, finally, according to Fig. 1f, the channel doping of the SOI MOSFET to be produced is brought about by a further implantation step. The channel implantation step is indicated by the arrows 10.

It is also stated on page 15 of the specification, line 12, that the implantation steps (Fig. 1b, Fig. 1f) can be carried out in a positionally selective manner by using non-illustrated implantation masks. In particular, the passivating

substance X can be implanted in a targeted manner for example only into n-channel transistors.

As set forth in the last paragraph on page 15 of the specification, line 18, the second method variant illustrated in Figs 2a to 2f differs from the first method variant shown in Figs 1a to 1f essentially merely in the fact that the implantation maximum 8 lies in the monocrystalline silicon layer 3 rather than in the buried oxide layer 2. In this case, the implanted dose of the passivating substance X should lie below the amorphizing dose in silicon. According to Fig. 2c, in this variant the implanted passivating substance X diffuses both to the interface 7 between buried oxide layer 2 and monocrystalline silicon layer 3 and to an interface 11 between monocrystalline silicon layer 3 and screen oxide layer 4. As a result, after removal of the screen oxide layer 4 and subsequent growth of a gate oxide layer on the monocrystalline silicon layer 3, the latter still contains sufficient passivating substance X in the region near the interface to increase the resistance of the gate oxide layer as well with respect to damage caused by hot charge carriers.

Appellants described on page 16 of the specification, line 10, that the steps of patterning/insulation, spacer formation and channel implantation as illustrated in Figs 2d to 2f are

carried out analogously to the steps illustrated in Figs 1d to 1f.

As further described on page 16 of the specification, line 15, the heat-treatment step shown in Fig. 2c may also be carried out after the Mesa insulation (Fig. 2d) and the provision of the spacers 9 (Fig. 2e). In that case, the passivating substance X is situated only in those portions of the interfaces 7, 11 which are covered by the layer regions 3', 4', i.e. in the active regions. When spacers 9 made of silicon oxide and a nitrogen passivating substance X are used, the spacer inner walls adjoining the peripheral walls of the layer regions 3', 4' are also nitrided in this case. During the subsequent channel doping (Fig. 2f) this inhibits the outdiffusion of channel dopant into the spacers and consequently suppresses the formation of Mesa sidewall transistors in a desired manner.

Appellants explained on page 17 of the specification, line 4, that halogens used as passivating substance X, on the other hand, accelerate the diffusion of channel dopant, in particular boron, into spacers 9 formed from silicon oxide. In order to avoid sidewall transistors, Mesa spacers 9 formed from silicon nitride are used in this case.

Appellants further explained on 17 of the specification, line 10, that, in the case of the third design variant of the method according to the invention as illustrated in Figs 3a to 3f, the passivating substance X is introduced into the buried oxide layer 2 as in the case of the first design variant (Figs 1a to f). The corresponding implantation step is illustrated in Fig. 3d. In contrast to the first design variant, however, the patterning/insulation and also the formation of the Mesa spacers 9 and subsequent thermal oxidation of the monocrystalline layer region 3' for the purpose of forming the screen layer region 4' (see Figs. 3a to 3c) eventually take place prior to the passivating substance implantation step in this case.

It is set forth in the last paragraph on page 17 of the specification, line 23, that, if the spacers 9 are composed of silicon oxide, the consequence of this is that the passivating substance X is also implanted into the Mesa spacers 9, since the implantation depth is smaller in silicon oxide than in monocrystalline silicon. As a result, the suppressing - which was described in the case of the second design variant - of Mesa sidewall transistors in the event of using nitrogen as passivating substance X takes place in this case as well. Fig. 3e shows the nitrogen distribution 8' resulting after the heat-treatment step in the region of the interface 7 and at

the peripheral walls of the monocrystalline layer region 3'. In the event of using halogens as passivating substance, spacers 9 composed of silicon nitride should be used - as already described in connection with the second design variant.

Appellants stated on page 18 of the specification, line 12, that Fig. 3f again shows the channel implantation step.

Appellants further stated on page 18 of the specification, line 14, that, if the heat-treatment step illustrated in Fig. 3e is not carried out until after the channel implantation (Fig. 3f), the well photomask (not illustrated) used for the channel implantation can be used to mask the implantation of the passivating substance X as well, with no additional outlay. In this procedure, too, the passivating substance X is implanted into the Mesa spacers 9, provided that the latter are composed of silicon oxide.

As set forth in the last paragraph on page 18 of the specification, line 23, Figs 4a to 4f show a fourth design variant of the method according to the invention. In this case, as in the case of the third design variant, the patterning/insulation, the Mesa spacer formation and the thermal oxidation of the active silicon layer region 3' (Figs

4a to 4c) take place before the introduction of the passivating substance X by an implantation step (Fig. 4d). In contrast to the third design variant, a lower implantation energy is chosen in this case, with the result that the implantation maximum 8 lies within the monocrystalline Si layer region 3'. Implantation into the spacers 9 takes place in this case as well. Fig. 4e shows the distribution 8' of the passivating substance X after the heat-treatment step. The advantage of this design variant resides in the additional passivation (halogenation or nitriding) of the gate oxide to be grown on later (cf. the second design variant as well) and - given the use of nitrogen implantation and oxide spacers 9 - in the nitriding of the Mesa spacer inner side for the purpose of suppressing Mesa sidewall transistors. Fig. 4e shows that the active monocrystalline silicon layer region 3' is completely passivated on all sides.

Appellants outlined on page 19 of the specification, line 18, that, if halogens are used as the passivating substance X, spacers 9 made of silicon nitride should again be used. In addition, as in the case of the third design variant, it is possible, during the masking of the passivating substance implantation step (Fig. 4d), to use the same mask as for the channel implantation step (Fig. 4f).

It is stated in the last paragraph on page 19 of the specification, line 25, that the table below shows the bond energies of silicon with hydrogen and also the passivating substances nitrogen, fluorine and chlorine. It is evident that the Si-X bond has a distinctly higher bond energy when the above-mentioned passivating substances X are used than when hydrogen is used as the bonding partner.

Table: Bond energies of silicon bonds

Bond	Bond Energy [eV]
Si-H	3.1
Si-N	4.6
Si-F	5.7
Si-Cl	4.7

References Cited:

U.S. Patent No. 5,468,657 (*Hsu*), dated November 21, 1995;

U.S. Patent No. 6,121,117 (*Sato et al.*), dated September 19, 2000.

Issues

Whether or not claims 16-21 and 23-25 are obvious over *Hsu* in view of *Sato et al.* under 35 U.S.C. §103. (Claim 22 has been held allowable by the Examiner, if rewritten or amended to

include all of the limitations of the base claim and any intervening claims.)

Grouping of Claims:

Claim 16 is independent. Claims 17-25 ultimately depend on claim 16. The patentability of the dependent claims 17-21 and 23-25 is not separately argued. Therefore, dependent claims 17-21 and 23-25 stand or fall with claim 16. (Claim 22 has only been objected to by the Examiner.)

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 16 calls for, inter alia:

> fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;
>
> ***placing*** a passivating substance X ***into*** the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and
>
> heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to

diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

In the *Response to Arguments* on page 7 of the Office action dated July 15, 2003, the Examiner stated that:

> As shown Fig. 4, as applicants correctly pointed out, Hsu et al. discloses an SOI substrate comprises the first layer (44) of monocrystalline silicon the second layer (59) of silicon oxide formed directly on the first layer and the third layer (42) of monocrystalline silicon. As figure 4 shows, the third layer (20) of the monocrystalline silicon layer is implanted with a nitrogen ion ("passivating substance") and the ***nitrogen penetrates through the third layer of monocrystalline silicon (20) and goes deep into the second layer of silicon oxide (59)*** (i.e., monocrystalline silicon also implanted). Therefore, Examiner respectfully submits that Hsu et al disclose introducing of "passivating substance", i.e., nitrogen ion, into a monocrystailine silicon layer.

(Emphasis added.)

Fig. 4 of *Hsu*, re-produced below, shows, as described in col. 7, lines 35-38, "a wafer 20 with an upper layer 42 of monocrystalline silicon, a middle layer 59 of nitrogen-implanted silicon dioxide, and a lower monocrystalline silicon 44."

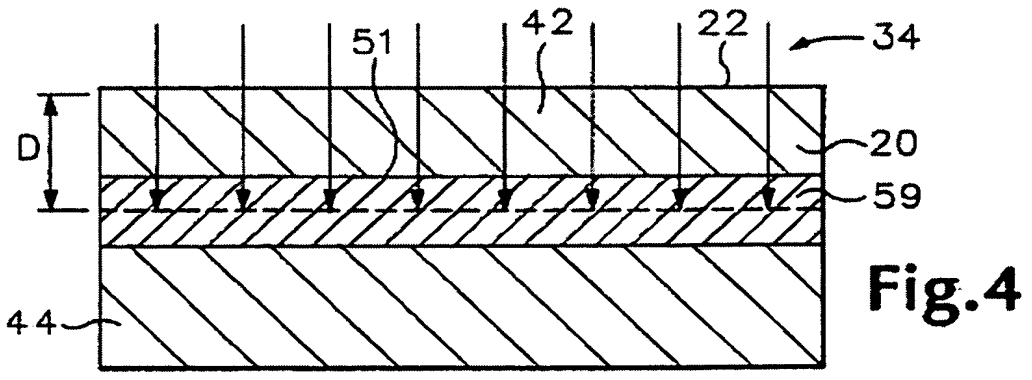


Fig.4

It is clear from Fig. 4 and from the specification of *Hsu* that in *Hsu* the nitrogen is ***placed*** into the ***silicon dioxide layer*** 59 (col. 1, lines 35-36) and is ***not*** placed into the monocrystalline silicon layer 42 or monocrystalline silicon layer 44. In contrast, in the invention of the instant application as recited in claim 16, the passivating substance is placed into the ***monocrystalline silicon layer***. Passing the nitrogen ***through*** the monocrystalline silicon layer 42 is not equivalent with placing the nitrogen ***into*** the monocrystalline silicon layer 42.

Furthermore, as can be clearly seen in Fig. 1D (similarly Fig. 3), re-produced below, the nitrogen diffuses within the ***silicon oxide layer*** 40 to the edges of the silicon oxide layer 40. In contrast, in the invention of the instant application as recited in claim 16, the passivating substance diffuses within the ***monocrystalline silicon layer***.

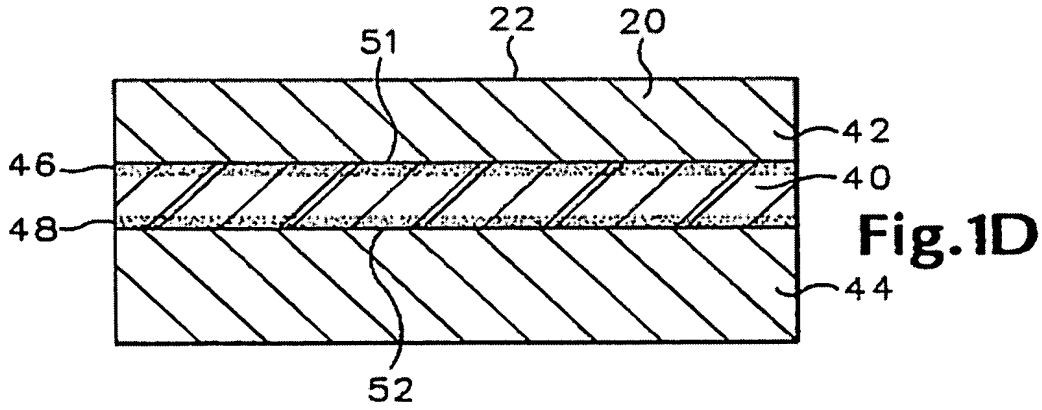


Fig.1D

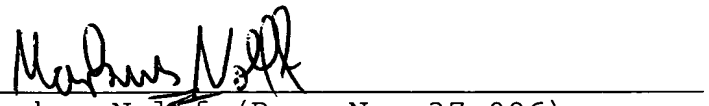
The inventive concept of the present invention is based on the underlying realization that after introducing and placing a passivating substance X into the monocrystalline silicon layer, heat-treating the semiconductor structure, removing the screen oxide layer, and subsequent growth of a gate oxide layer on the monocrystalline silicon layer, the monocrystalline silicon layer still contains sufficient passivating substance X to increase the resistance of the gate oxide layer to damage caused by hot charge carriers. There is no disclosure or suggestion in either *Hsu* or *Sato et al.* to introduce and place a passivating substance into a monocrystalline silicon layer. Furthermore, neither *Hsu* nor *Sato et al.* contain teachings that would suggest the underlying realization on which the present invention is based. Therefore, the invention as recited in claim 16 of the instant application is believed not to be obvious over *Hsu* in view of *Sato et al.*.

It is accordingly believed to be clear that *Hsu* in view of *Sato et al.* do not suggest the features of claim 16. Claim 16 is, therefore, believed to be patentable over the art and since claims 17-21 and 23-25 are ultimately dependent on claim 16, they are believed to be patentable as well. (Claim 22 has been held allowable by the Examiner, if rewritten or amended

to include all of the limitations of the base claim and any intervening claims.)

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,



Markus Nolff (Reg. No. 37,006)

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Appendix - Appealed Claims:

16. A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

17. The method according to claim 16, wherein the introducing step comprises ion-implanting the passivating substance X.

18. The method according to claim 17, wherein the introducing step is performed such that there is an

implantation concentration maximum for the passivating substance X in the vicinity of the interface.

19. The method according to claim 16, wherein the fabricating of the semiconductor structure comprises the following steps:

providing two silicon semiconductor substrates;

oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and

partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer.

20. The method according to claim 16, which comprises forming a covering oxide layer on the monocrystalline silicon layer.

21. The method according to claim 16, which comprises patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer.

23. The method according to claim 21, wherein the patterning step is performed after the step of introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer.

24. The method according to claim 16, which comprises:

doping the monocrystalline silicon layer differently region by region by ion implantation; and

performing the doping step after the step of introducing the passivating substance X and the heat-treating step.

25. The method according to claim 21, wherein the step of introducing a passivating substance X into the monocrystalline silicon layer is performed such that an implanted dose of the passivating substance X is below an amorphizing dose of silicon.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

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Appellants described on page 14 of the specification, line 12, that Figs 1d to 1f show, by way of example, further process steps which are carried out for the patterning and insulation of the monocrystalline silicon layer 3 for the purpose of forming an SOI MOSFET. Such steps are also necessary to construct an integrated CMOS circuit on the SOI semiconductor structure 5. First of all, in accordance with Fig. 1d, the screen oxide layer 4 and the monocrystalline silicon layer 3

are removed, except for locally residual layer regions 3', 4', using customary photolithographic masking techniques and etching steps. As a result, the monocrystalline layer region 3' is electrically insulated from corresponding, adjacent layer regions (not illustrated in Fig. 1d). The method shown here is known as Mesa insulation in the art. Other insulation methods (for example LOCOS, STI) can also be employed instead of Mesa insulation.

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As set forth in the last paragraph on page 15 of the specification, line 18, the second method variant illustrated in Figs 2a to 2f differs from the first method variant shown in Figs 1a to 1f essentially merely in the fact that the implantation maximum 8 lies in the monocrystalline silicon layer 3 rather than in the buried oxide layer 2. In this case, the implanted dose of the passivating substance X should lie below the amorphizing dose in silicon. According to Fig. 2c, in this variant the implanted passivating substance X diffuses both to the interface 7 between buried oxide layer 2 and monocrystalline silicon layer 3 and to an interface 11 between monocrystalline silicon layer 3 and screen oxide layer 4. As a result, after removal of the screen oxide layer 4 and subsequent growth of a gate oxide layer on the monocrystalline silicon layer 3, the latter still contains sufficient passivating substance X in the region near the interface to increase the resistance of the gate oxide layer as well with respect to damage caused by hot charge carriers.

Appellants described on page 16 of the specification, line 10, that the steps of patterning/insulation, spacer formation and channel implantation as illustrated in Figs 2d to 2f are

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As further described on page 16 of the specification, line 15, the heat-treatment step shown in Fig. 2c may also be carried out after the Mesa insulation (Fig. 2d) and the provision of the spacers 9 (Fig. 2e). In that case, the passivating substance X is situated only in those portions of the interfaces 7, 11 which are covered by the layer regions 3', 4', i.e. in the active regions. When spacers 9 made of silicon oxide and a nitrogen passivating substance X are used, the spacer inner walls adjoining the peripheral walls of the layer regions 3', 4' are also nitrided in this case. During the subsequent channel doping (Fig. 2f) this inhibits the outdiffusion of channel dopant into the spacers and consequently suppresses the formation of Mesa sidewall transistors in a desired manner.

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It is set forth in the last paragraph on page 17 of the specification, line 23, that, if the spacers 9 are composed of silicon oxide, the consequence of this is that the passivating substance X is also implanted into the Mesa spacers 9, since the implantation depth is smaller in silicon oxide than in monocrystalline silicon. As a result, the suppressing - which was described in the case of the second design variant - of Mesa sidewall transistors in the event of using nitrogen as passivating substance X takes place in this case as well. Fig. 3e shows the nitrogen distribution 8' resulting after the heat-treatment step in the region of the interface 7 and at

the peripheral walls of the monocrystalline layer region 3'. In the event of using halogens as passivating substance, spacers 9 composed of silicon nitride should be used - as already described in connection with the second design variant.

Appellants stated on page 18 of the specification, line 12, that Fig. 3f again shows the channel implantation step.

Appellants further stated on page 18 of the specification, line 14, that, if the heat-treatment step illustrated in Fig. 3e is not carried out until after the channel implantation (Fig. 3f), the well photomask (not illustrated) used for the channel implantation can be used to mask the implantation of the passivating substance X as well, with no additional outlay. In this procedure, too, the passivating substance X is implanted into the Mesa spacers 9, provided that the latter are composed of silicon oxide.

As set forth in the last paragraph on page 18 of the specification, line 23, Figs 4a to 4f show a fourth design variant of the method according to the invention. In this case, as in the case of the third design variant, the patterning/insulation, the Mesa spacer formation and the thermal oxidation of the active silicon layer region 3' (Figs

4a to 4c) take place before the introduction of the passivating substance X by an implantation step (Fig. 4d). In contrast to the third design variant, a lower implantation energy is chosen in this case, with the result that the implantation maximum 8 lies within the monocrystalline Si layer region 3'. Implantation into the spacers 9 takes place in this case as well. Fig. 4e shows the distribution 8' of the passivating substance X after the heat-treatment step. The advantage of this design variant resides in the additional passivation (halogenation or nitriding) of the gate oxide to be grown on later (cf. the second design variant as well) and - given the use of nitrogen implantation and oxide spacers 9 - in the nitriding of the Mesa spacer inner side for the purpose of suppressing Mesa sidewall transistors. Fig. 4e shows that the active monocrystalline silicon layer region 3' is completely passivated on all sides.

Appellants outlined on page 19 of the specification, line 18, that, if halogens are used as the passivating substance X, spacers 9 made of silicon nitride should again be used. In addition, as in the case of the third design variant, it is possible, during the masking of the passivating substance implantation step (Fig. 4d), to use the same mask as for the channel implantation step (Fig. 4f).

It is stated in the last paragraph on page 19 of the specification, line 25, that the table below shows the bond energies of silicon with hydrogen and also the passivating substances nitrogen, fluorine and chlorine. It is evident that the Si-X bond has a distinctly higher bond energy when the above-mentioned passivating substances X are used than when hydrogen is used as the bonding partner.

Table: Bond energies of silicon bonds

Bond	Bond Energy [eV]
Si-H	3.1
Si-N	4.6
Si-F	5.7
Si-Cl	4.7

References Cited:

U.S. Patent No. 5,468,657 (*Hsu*), dated November 21, 1995;

U.S. Patent No. 6,121,117 (*Sato et al.*), dated September 19, 2000.

Issues

Whether or not claims 16-21 and 23-25 are obvious over *Hsu* in view of *Sato et al.* under 35 U.S.C. §103. (Claim 22 has been held allowable by the Examiner, if rewritten or amended to

include all of the limitations of the base claim and any intervening claims.)

Grouping of Claims:

Claim 16 is independent. Claims 17-25 ultimately depend on claim 16. The patentability of the dependent claims 17-21 and 23-25 is not separately argued. Therefore, dependent claims 17-21 and 23-25 stand or fall with claim 16. (Claim 22 has only been objected to by the Examiner.)

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 16 calls for, inter alia:

> fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;
>
> ***placing*** a passivating substance X ***into*** the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and
>
> heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to

diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

In the *Response to Arguments* on page 7 of the Office action dated July 15, 2003, the Examiner stated that:

> As shown Fig. 4, as applicants correctly pointed out, Hsu et al. discloses an SOI substrate comprises the first layer (44) of monocrystalline silicon the second layer (59) of silicon oxide formed directly on the first layer and the third layer (42) of monocrystalline silicon. As figure 4 shows, the third layer (20) of the monocrystalline silicon layer is implanted with a nitrogen ion ("passivating substance") and the ***nitrogen penetrates through the third layer of monocrystalline silicon (20) and goes deep into the second layer of silicon oxide (59)*** (i.e., monocrystalline silicon also implanted). Therefore, Examiner respectfully submits that Hsu et al disclose introducing of "passivating substance", i.e., nitrogen ion, into a monocrystailine silicon layer.

(Emphasis added.)

Fig. 4 of *Hsu*, re-produced below, shows, as described in col. 7, lines 35-38, "a wafer 20 with an upper layer 42 of monocrystalline silicon, a middle layer 59 of nitrogen-implanted silicon dioxide, and a lower monocrystalline silicon 44."

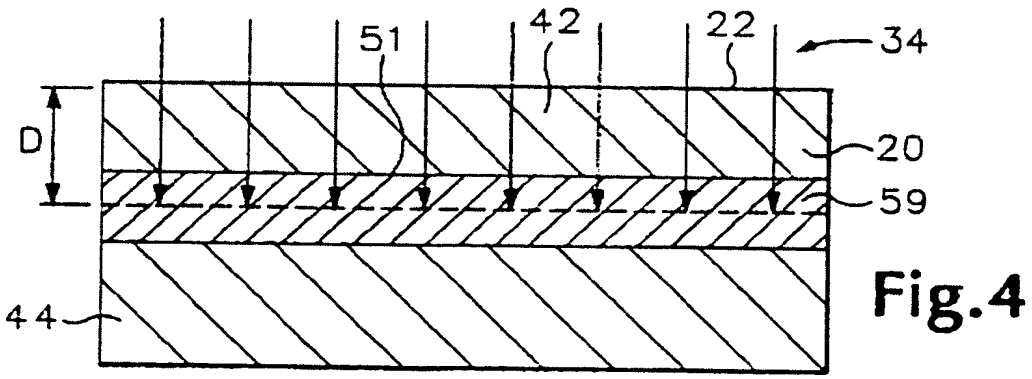


Fig.4

It is clear from Fig. 4 and from the specification of *Hsu* that in *Hsu* the nitrogen is ***placed*** into the ***silicon dioxide layer*** 59 (col. 1, lines 35-36) and is ***not*** placed into the monocrystalline silicon layer 42 or monocrystalline silicon layer 44. In contrast, in the invention of the instant application as recited in claim 16, the passivating substance is placed into the ***monocrystalline silicon layer***. Passing the nitrogen ***through*** the monocrystalline silicon layer 42 is not equivalent with placing the nitrogen ***into*** the monocrystalline silicon layer 42.

Furthermore, as can be clearly seen in Fig. 1D (similarly Fig. 3), re-produced below, the nitrogen diffuses within the ***silicon oxide layer*** 40 to the edges of the silicon oxide layer 40. In contrast, in the invention of the instant application as recited in claim 16, the passivating substance diffuses within the ***monocrystalline silicon layer***.

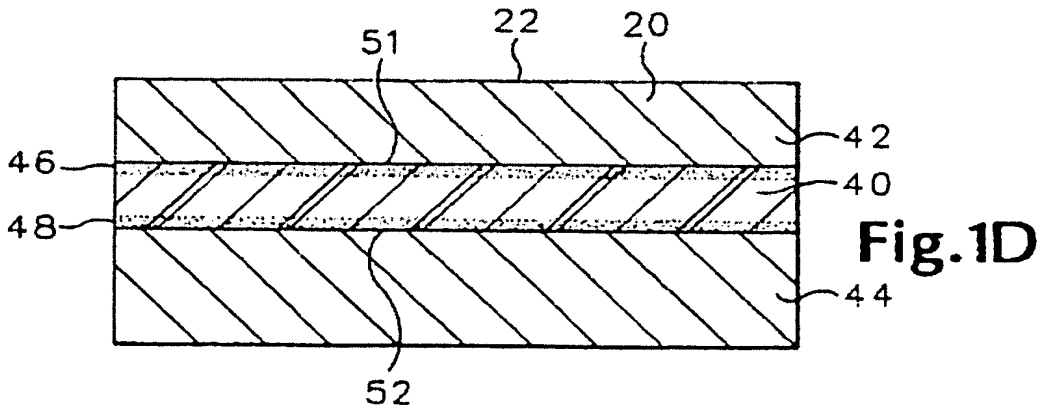


Fig.1D

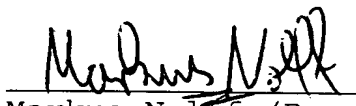
The inventive concept of the present invention is based on the underlying realization that after introducing and placing a passivating substance X into the monocrystalline silicon layer, heat-treating the semiconductor structure, removing the screen oxide layer, and subsequent growth of a gate oxide layer on the monocrystalline silicon layer, the monocrystalline silicon layer still contains sufficient passivating substance X to increase the resistance of the gate oxide layer to damage caused by hot charge carriers. There is no disclosure or suggestion in either *Hsu* or *Sato et al.* to introduce and place a passivating substance into a monocrystalline silicon layer. Furthermore, neither *Hsu* nor *Sato et al.* contain teachings that would suggest the underlying realization on which the present invention is based. Therefore, the invention as recited in claim 16 of the instant application is believed not to be obvious over *Hsu* in view of *Sato et al.*.

It is accordingly believed to be clear that *Hsu* in view of *Sato et al.* do not suggest the features of claim 16. Claim 16 is, therefore, believed to be patentable over the art and since claims 17-21 and 23-25 are ultimately dependent on claim 16, they are believed to be patentable as well. (Claim 22 has been held allowable by the Examiner, if rewritten or amended

to include all of the limitations of the base claim and any intervening claims.)

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,



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Appendix - Appealed Claims:

16. A method of fabricating a semiconductor configuration, which comprises the following steps:

fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

placing a passivating substance X into the monocrystalline silicon layer, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X in the monocrystalline silicon layer to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

17. The method according to claim 16, wherein the introducing step comprises ion-implanting the passivating substance X.

18. The method according to claim 17, wherein the introducing step is performed such that there is an

implantation concentration maximum for the passivating substance X in the vicinity of the interface.

19. The method according to claim 16, wherein the fabricating of the semiconductor structure comprises the following steps:

providing two silicon semiconductor substrates;

oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and

partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer.

20. The method according to claim 16, which comprises forming a covering oxide layer on the monocrystalline silicon layer.

21. The method according to claim 16, which comprises patterning the monocrystalline silicon layer by etching away regions thereof down to the underlying insulation layer.

23. The method according to claim 21, wherein the patterning step is performed after the step of introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer.

24. The method according to claim 16, which comprises:

doping the monocrystalline silicon layer differently region by region by ion implantation; and

performing the doping step after the step of introducing the passivating substance X and the heat-treating step.

25. The method according to claim 21, wherein the step of introducing a passivating substance X into the monocrystalline silicon layer is performed such that an implanted dose of the passivating substance X is below an amorphizing dose of silicon.